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High-Pressure H_2O Vapor Heat Treatment Used to Fabricate Poly-Si Thin Film Transistors

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High-pressure H_2O vapor heat treatment was applied to reduction of defect states of silicon films and SiO_x/Si interfaces in the fabrication of n-channel polycrystalline silicon thin film transistors (poly-Si TFTs). A carrier mobility of 170 $cm^2/V{\cdot}s$ and a low threshold voltage of 2.4 V were achieved by heat treatment at 260°C with 1.3×10^6 Pa H_2O vapor for 3 h applied to 25-nm-thick silicon films crystallized by the irradiation of a 30-ns-pulsed XeCl excimer laser at 280 mJ/cm^2. Additional high-pressure H_2O vapor heat treatment after TFT fabrication further improved them to 620 $cm^2/V{\cdot}s$ and 1.7 V, respectively. [DOI: 10.1143/JJAP.41.L974]

KEYWORDS: laser crystallization, defect states, mobility, threshold voltage

Low-temperature fabrication of polycrystalline silicon films formed by pulsed laser crystallization is attractive for electron device fabrication, such as thin-film transistors (TFTs) and solar cells, because crystallization occurs rapidly and no thermal damage is induced in a cheap substrate such as glass.[1–4] However, rapid laser annealing causes a large amount of defect states at grain boundaries. Therefore, defect reduction technologies at low temperature is very important. Many investigations such as plasma hydrogenation have been reported for defect reduction.[5–10] We have recently reported the improvement of electrical properties of laser crystallized silicon films by a simple heat treatment with high-pressure H_2O vapor.[11–14] Defect states are changed to electrically inactive by a reaction with oxygen atoms.

In this paper, we report the application of heat treatment with high-pressure H_2O vapor in order to improve the characteristics of poly-Si TFTs. We show that high-pressure H_2O vapor treatments reduced the density of defect states in silicon films as well as SiO_x gate insulators. The defect reduction results in a low threshold voltage and a high drain current with a high carrier mobility. We also analyze the relation between the density of defects and the characteristics of poly-Si TFTs.

Figure 1 shows the schematic fabrication steps of poly-Si TFTs. Hydrogenated amorphous silicon (a-Si:H) films doped with 7×10^{20} cm^{-3}-phosphorus and with a thickness of 30 nm were first formed on glass substrates at 330°C using plasma enhanced chemical vapor deposition (PECVD). The doped films were removed at channel region with a length of 25 μm by etching and they were used as dopant sources for forming source and drain regions. A 25-nm-thick undoped a-Si:H films were then deposited using PECVD over the whole area. The silicon layers were crystallized at 250°C in vacuum at 3×10^{-4} Pa by 30-ns-pulsed XeCl excimer laser with energy densities of 280 mJ/cm^2 and 50 shots. Undoped crystallized regions were used as channel regions. Source and drain regions were simultaneously formed through diffusion of phosphorus atoms into the overlaying silicon layer during the laser crystallization. The melt duration of silicon during laser crystallization was shorter than 100 ns so that the diffusion distance of the dopant atom was at most 60 nm in liquid silicon[15] and the 25-μm channel length hardly changed. After laser crystallization, the silicon films were annealed at 260°C with 1.3×10^6 Pa H_2O vapor for 3 h for defect reduction in polycrystalline silicon films. The silicon films were then patterned by etching for isolation. The molecular beam deposition method was used for formation of the gate insulator. An 120-nm-thick SiO_x layer was deposited at room temperature as the gate insulator by thermal evaporation of SiO powders using a Knudsen cell in oxygen radicals at 1×10^{-2} Pa, which was generated by 300 W induction coupled remote plasma equipment.[16] Contact holes were then opened in the SiO_x layer on the source and drain regions. Gate, drain and source electrodes were formed with Al metals. After TFT fabrication, some samples were also annealed at 260°C with 1.3×10^6 Pa H_2O vapor for 3 h for defect reduction in SiO_x

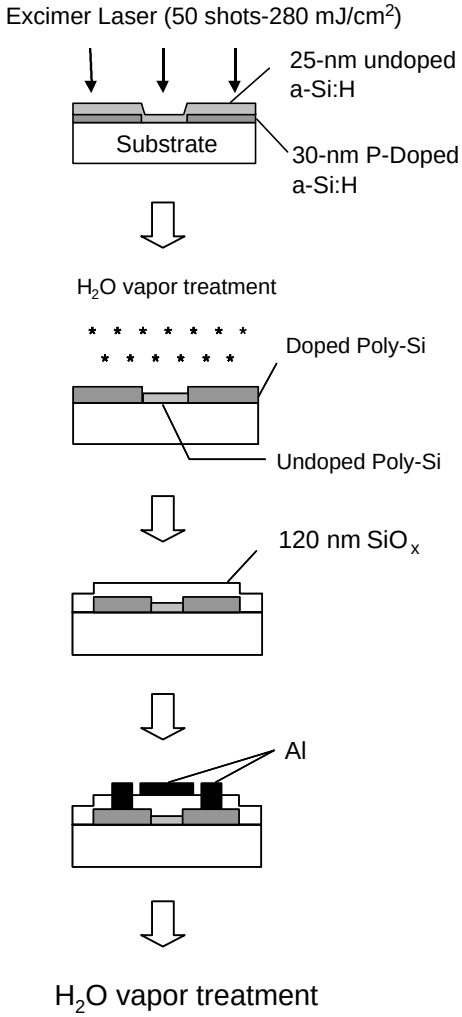

Fig. 1. Schematic fabrication steps of poly-Si TFTs.

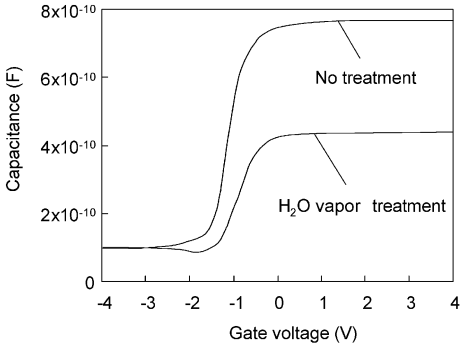

Fig. 2. Capacitance vs voltage characteristics with high frequency at 1 MHz for Al-gate MOS capacitors with 120-nm-thick SiO_x films for n-type substrates fabricated by thermal evaporation of SiO powders at room temperature in oxygen radicals. The area of the Al electrodes is 0.01 cm^2. High-pressure H_2O vapor heat treatment was carried out at 260°C and 1.3 MPa for 3 h.

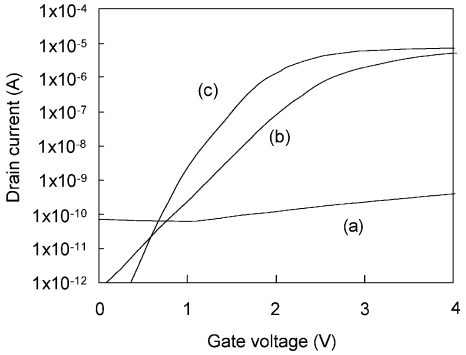

Fig. 3. Transfer characteristics for TFTs fabricated with no H_2O vapor heat treatment (a), H_2O vapor heat treatment after laser crystallization (b) and additional H_2O vapor heat treatment after TFT fabrication (c).

as well as SiO_x/Si interfaces. Figure 2 shows the capacitance responses with the gate voltage with frequencies of 1 MHz for Al gate metal-oxide-semiconductor (MOS) capacitors with the present SiO_x formed on n-type crystalline silicon with a bulk-carrier density of 5×10^{14} cm^{-3} for as-fabricated and annealed at 260°C with 1.3×10^6 Pa H_2O vapor for 3 h. A sharp capacitance transition was observed. From the curve of capacitance versus gate voltage, the specific dielectric constant of the SiO_x layer, the densities of interface traps and fixed oxide charges were estimated to be 8.7, 3.9×10^{11} $cm^{-2}\cdot eV^{-1}$ and 4.5×10^{11} cm^{-2}, respectively, for as-fabricated MOS capacitors when the work function of Al gate metal was 4.3 eV. The high specific dielectric constant of 8.7 results from the high dielectric-dispersion characteristic in the low frequency regime compared with that of thermally grown SiO_2, while the specific dielectric constant of the SiO_x layer was 2.16 in the visible-wavelength range, which was almost the same as that of thermally grown SiO_2. The high dielectric-dispersion characteristic was probably caused by bonding distortion of Si–O associated with the lack of oxygen atoms in the SiO_x films.[13] H_2O vapor heat treatment oxidized the SiO_x films well and reduced the maximum oxide capacitance associated with reduction of the specific dielectric constant. The C–V curves were shifted to the positive gate voltage direction because of a reduction of the density of fixed oxide charges. A sharp capacitance transition was also observed after the high-pressure H_2O vapor heat treatment. This means that the interface trap states were occupied by a small amount of charges accumulated at the SiO_x/Si interface caused by gate voltage application with the low oxide capacitance. The specific dielectric constant of the SiO_x layer, the densities of interface traps and fixed oxide charges were estimated to be 4.9, 2×10^{10} $cm^{-2}\cdot eV^{-1}$ and 1.7×10^{11} cm^{-2}, respectively.

Figure 3 shows transfer characteristics of TFTs fabricated at 280 mJ/cm^2-laser crystallization with no H_2O vapor heat treatments (a), H_2O vapor heat treatment applied to silicon films (b), and additional H_2O vapor heat treatment after TFT fabrication (c). TFTs had a gate width of 80 μm and a gate length of 25 μm. The transfer characteristics were measured at a drain voltage 0.1 V. Very low drain current with a high threshold voltage was measured for TFTs with no H_2O vapor heat treatments, as shown by curve (a) in Fig. 3. This means that highly dense defect states in the channel region of polycrystalline silicon made the density of free electrons low because of carrier trap under the gate voltage application ranging from 0 to 4 V. On the other hand, a sharp increase in the drain current was observed for TFT with H_2O vapor heat treatment to silicon films, as shown by curve (b) in Fig. 3. The threshold voltage, V_t, and the effective carrier mobility, μ, were estimated from the linear relation between gate voltage and drain current, as follows.

$$V_t = V_g - \frac{V_d}{2} - I_d \left(\frac{\partial I_d}{\partial V_g} \right)^{-1}$$

$$\mu = \left(\frac{W}{L} C_{ox} V_d \right)^{-1} \frac{\partial I_d}{\partial V_g} \qquad (1)$$

where V_g and V_d are the gate voltage and the drain voltage, respectively, I_d is the drain current, W and L are the gate width and the gate length and C_{ox} is the gate capacitance, which was obtained from C–V measurements. The threshold voltage and the effective carrier mobility were 2.4 V and 170 $cm^2/V\cdot s$ at maximum, respectively. H_2O vapor heat treatment effectively changed the defect states to electrically inactive and made the channel region conductive under the low gate voltage application. The additional high-pressure H_2O vapor heat treatment after TFT fabrication further improved the characteristics of TFTs, as shown by curve (c) in Fig. 3. The threshold voltage decreased to 1.7 V. The peak effective carrier mobility increased to 620 $cm^2/V\cdot s$ at a gate voltage of 2.3 V.

In order to estimate the density of defect states in polycrystalline silicon films as well as SiO_2/Si interfaces, transfer characteristics were analyzed using a numerical calculation program, which was constructed with the finite-element method combined with statistical thermodynamical conditions with defect states localized at SiO_2/Si interfaces as well as silicon films.[17,18] We introduced the deep-level defect states localized at the mid gap, which had a Gaussian-type energy distribution. Tail-state-type defect states were also introduced symmetrically in the band gap. The density exponentially decreased from the conduction band as well as valence band edges to a deep energy level in the band gap. The defect states were placed uniformly in the silicon films. One half of the defect states was occupied by electrons in the flat band condition. Poly-Si TFTs had another density of defect states at SiO_x/poly-Si interfaces. We assumed that the interface defect states were generated at SiO_x film formation. In the present analysis, we used the density of interface traps

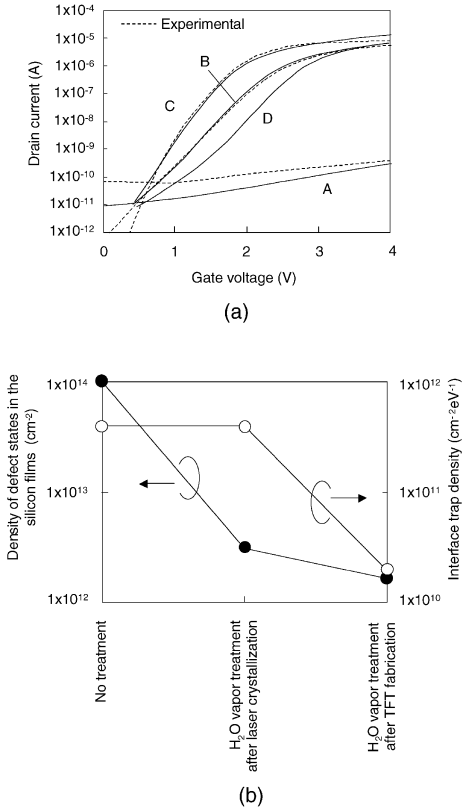

Fig. 4. (a) Calculated drain current for TFTs fabricated with no H_2O vapor heat treatment, curve A, H_2O vapor heat treatment after laser crystallization, curve B, and additional H_2O vapor heat treatment after TFT fabrication, curve C. Curve D is the calculated transfer characteristics with initial density of interface traps and with density of defect states in the silicon films same as that of curve C. The dashed curves were experimental drain currents. Figure 4(b) shows the density of unoccupied defect states at the flat band condition in the silicon films and interface trap density as a function of defect reduction sequence. Interface trap density was obtained by *C–V* measurement.

which was obtained by *C–V* measurements of MOS capacitors. The carrier mobility was also calculated with effects of impurity scattering and lattice scattering depending on the electrical field caused by gate voltage application.[19,20] The best agreement of calculated transfer characteristics to experimental ones resulted in the density of defect states. Figure 4(a) shows calculated curves of the drain current as a function of the gate voltage. The dashed curves were experimental drain currents as shown in Fig. 3. For calculation, the density of tail states at the band edge of the silicon films, the width of the states and the density of defects at the mid gap were $2 \times 10^{14}\,cm^{-2}\cdot eV^{-1}$, 0.5 eV and $6.5 \times 10^{13}\,cm^{-2}\cdot eV^{-1}$ for curve A, $2.5 \times 10^{13}\,cm^{-2}\cdot eV^{-1}$, 0.07 eV and $9.0 \times 10^{11}\,cm^{-2}\cdot eV^{-1}$ for curve B, and $2.5 \times 10^{13}\,cm^{-2}\cdot eV^{-1}$, 0.04 eV and $3.0 \times 10^{11}\,cm^{-2}\cdot eV^{-1}$ for curve C, respectively. Those were the densities of the unoccupied states in the flat band condition. Although the calculated drain current of curve A did not fit the experimental one well in the case of TFTs with no H_2O vapor heat treatment, the calculation suggested that the silicon films that crystallized at $280\,mJ/cm^2$ had a high density of defect states of $1 \times 10^{14}\,cm^{-2}$, as shown in Fig. 4(b). The curve B is a calculated drain current, which was well fitted to the experimental drain current for H_2O vapor heat treatment applied to only silicon films. The calculation revealed that the density of defect states in the silicon films was reduced to $3.2 \times 10^{12}\,cm^{-2}$ by the H_2O vapor heat treatment applied to silicon films, as shown in Fig. 4(b). The transfer characteristics for TFTs fabricated with the additional H_2O vapor heat treatment was agreed well with curve C, which was calculated with the density of defect states at SiO_2/Si of $2 \times 10^{10}\,cm^{-2}\cdot eV^{-1}$ obtained by *C–V* measurements, and with a density of defects states in the silicon films of $1.6 \times 10^{12}\,cm^{-2}$, as shown in Fig. 4(b). The defect density in the silicon films was further reduced by the additional H_2O vapor heat treatment. Curve D is an interesting demonstration. It was calculated drain current with the density of defect states at SiO_2/Si of $3.9 \times 10^{11}\,cm^{-2}\cdot eV^{-1}$ (the initial density of interface traps) and the SiO_x specific dielectric constant of 4.9 (H_2O vapor annealing case), and with the density of defect states in the silicon films of $1.6 \times 10^{12}\,cm^{-2}$ (the additional H_2O vapor annealing case). The drain current of curve D for the gate voltage ranging from 1 to 2.5 V was almost two orders of magnitude lower than that of curve C. The density of defect states at the SiO_x/Si interfaces is sensitive to the carrier density because the inversion layer is formed near the interfaces. The drain current was markedly increased by reduction of the density of interface defect states. The high drain current was achieved by reduction of the density of interface traps caused by the additional high-pressure H_2O vapor heat treatment, although the specific dielectric constant of SiO_x decreased from 8.7 to 4.9 after H_2O vapor annealing. The results in Fig. 4 clearly demonstrate the role of high-pressure H_2O vapor heat treatment for defect reduction. The reduction of the defect density in the silicon films to the order of $10^{12}\,cm^{-2}$ is first essential to improve the transfer characteristics because of the very high density of defect states of $1 \times 10^{14}\,cm^{-2}$ in as-crystallized silicon films. The density of defect states at the SiO_x/Si interfaces is then serious to transfer characteristics when the defect density in silicon films is reduced to a sufficiently low level. The high-pressure H_2O vapor heat treatment is effective to reduce the density of defect states at the SiO_x/Si interfaces although there are multiple layers of SiO_x and metal electrodes overlaying the silicon films. The combination of the high-pressure H_2O vapor heat treatment resulted in the high effective mobility of $620\,cm^2/V\cdot s$. The high effective mobility was obtained at a low electrical field of 9.5×10^4 V/cm at the interface in the depth direction, which was estimated with our analysis program. A high inversion mobility at the low electrical field appeared in the transfer characteristics because a high effective carrier density is achieved at the SiO_x/Si interfaces by low gate voltage application associated with the low density of defect states.

In summary, high-pressure H_2O vapor heat treatment was investigated in order to reduce defect states of silicon films and SiO_x films in the fabrication of n-channel polycrystalline silicon thin film transistors (poly-Si TFTs). Heat treatment at 260°C with 1.3×10^6 Pa H_2O vapor for 3 h was applied after crystallization of 25-nm-thick silicon films by 30 ns-pulsed XeCl excimer laser at $280\,mJ/cm^2$. It was also applied after TFT fabrication. The 120-nm-thick SiO_x gate insulator was formed at room temperature by molecular beam deposition at 10^{-2} Pa oxygen atmosphere including oxygen radicals. *C–V* measurements for MOS capacitors revealed a density of interface traps of $3.9 \times 10^{11}\,cm^{-2}\cdot eV^{-1}$. The first H_2O vapor heat treatment increased the drain current. A carrier mobil-

ity of 170 $cm^2/V{\cdot}s$ and a low threshold voltage of 2.4 V were achieved. Additional high-pressure H_2O vapor heat treatment after TFT fabrication further improved them to 620 $cm^2/V{\cdot}s$ and 1.7 V, respectively. Change in the defect states was investigated using a numerical analysis. The density of defect states in the crystallized silicon films was reduced from $1 \times 10^{14}\,cm^{-2}$ (as crystallized) to $3.2 \times 10^{12}\,cm^{-2}$ by the H_2O vapor heat treatment applied to the silicon films. It was further reduced to $1.6 \times 10^{12}\,cm^{-2}$ by the additional H_2O vapor heat treatment after TFT fabrication. The additional H_2O vapor heat treatment also improved the properties of the SiO_x/Si interface. The C–V measurements revealed that the density of interface traps was reduced to $2 \times 10^{10}\,cm^{-2}{\cdot}eV^{-1}$. The reduction of the densities of defect states in the silicon films and SiO_x/Si interface resulted in the high drain current at low gate voltages.

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