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# Current-Induced Joule Heating Used to Crystallize Silicon Thin Films

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Electrical-current-induced joule heating was applied to the crystallization of 60-nm-thick amorphous silicon films formed on glass substrates. Three-$\mu$s-pulsed voltages were applied to silicon films connected with a capacitance in parallel. Coincident irradiation with a 28-ns-pulsed excimer laser melted films partially and reduced their resistance. Complete melting for 12 $\mu$s and a low cooling rate of $1.1 \times 10^8$ K/s were achieved by joule heating from electrical energy that accumulated at a capacitance of 0.22 $\mu$F. The analysis of electrical conductivity suggested a density of defect states of $1.5 \times 10^{12}$ cm$^{-2}$ at grain boundaries. The formation of 3.5-$\mu$m-long crystalline grains was observed using a transmission electron microscope. The preferential crystalline orientation was (110).

KEYWORDS: joule heating, melt duration, cooling rate, electrical conductivity, grain boundary

Polycrystalline silicon films have been applied to many devices such as thin film transistors (TFTs) and solar cells.[1–6] The formation of polycrystalline silicon films at low cost has been demanded in recent years for the fabrication of large-area devices. Many technologies have been reported for the formation of polycrystalline silicon films at low processing temperatures.[1–10] The pulsed laser crystallization method has an advantage for the formation high-quality polycrystalline silicon films because of rapid melting followed by solidification. This method has therefore been applied to the fabrication of poly-Si TFTs and their electronic circuits. However, it is important to fabricate large crystalline grains with a low density of defect states, especially for solar cell application. Although several methods have been reported for the formation of large crystalline grains using the pulsed laser crystallization method,[11–13] it is not easy to control the solidification parameters such as crystallization velocity, cooling rate and solidification duration because the laser pulse is too short to control solidification temperature during the crystallization process.

In this paper, we propose a crystallization method involving pulsed-electrical current-induced heating of silicon films in order to fabricate large crystalline grains. We report that silicon thin films are melted for a long time and their melt duration is easily controlled by electrical current intensity. Large grain growth of 3.5 $\mu$m is demonstrated. Electrical properties of the crystalline grains and grain boundaries are analyzed and a low density of defect states is demonstrated.

Undoped 60-nm-thick amorphous silicon films were formed by low pressure chemical vapor deposition (LPCVD) methods on quartz glass substrates. Some silicon films were doped with phosphorus atoms at $7.4 \times 10^{17}$ cm$^{-3}$ using the ion implantation method. Undoped and lightly doped silicon strips with a width of 50 $\mu$m were defined by lithography and etching methods. Al electrodes with a gap of 250 $\mu$m were formed on the silicon strips. Samples were placed in a vacuum chamber and metal probes were connected to Al electrodes to apply electrical voltages to the silicon films. A voltage source generating pulsed voltages with a pulse width of 3 $\mu$s was used to heat the silicon films. Pulsed voltages were applied to the samples via simple electrical circuits with a series resistance, resistance of silicon and load resistance, as shown in the inset of Fig. 1. Simultaneous with voltage application, samples were irradiated by a 28-ns-pulsed XeCl excimer laser to melt the silicon films partially during voltage application. Because of an experimental system delay, laser pulses were irradiated on samples about 2.1 $\mu$s after the initiation of pulsed voltage application. Although silicon films have high resistivity in the solid phase at room temperature because of a low carrier density, the resistance of silicon markedly decreases when it is melted, because liquid silicon has a metallic phase. Laser-induced melting during voltage application therefore leads to a high joule heating per unit area induced by the electrical current, $I^2 R_{Si}/S$, where $S$ is area (width $\times$ length) of silicon films. The electrical current was measured as a voltage at a load resistance connected between sample and ground using a high-speed digital oscilloscope. Figure 1 shows changes in the electrical current flowing in silicon films with time. The samples were heated with only laser irradiation at 400 mJ/cm$^2$ as well as with laser irradiation at 400 mJ/cm$^2$ during application of a pulsed voltage at 110 V. A small current peak was observed for a very short period ($\sim$50 ns) for only laser irradiation at 400 mJ/cm$^2$ due to laser induced rapid melting of silicon films. On the other hand, a longer melting time was observed when silicon was subjected to a pulsed voltage at 110 V as well as laser irradiation, as shown in Fig. 1. The high current of $\sim$3 A almost leveled off until the termination of pulsed voltage. This means that the silicon films were completely melted and the resistance was limited by the resistivity of liquid silicon.

In order to melt silicon films for a longer time than the volt-

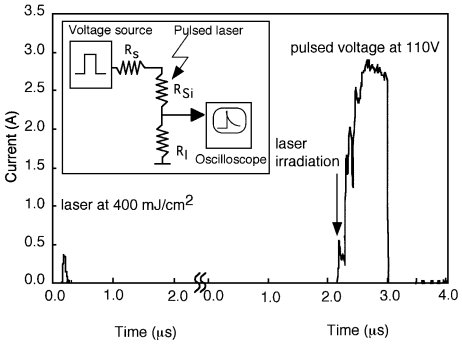


Fig. 1. Changes in the electrical current in silicon. The samples were heated with only laser irradiation at 400 mJ/cm$^2$ as well as with laser irradiation at 400 mJ/cm$^2$ during application of a 3 $\mu$s pulsed voltage at 110 V. The equivalent circuit is shown in the inset. Series resistance $R_s$ and load resistance $R_l$ were 4.0 and 4.8 $\Omega$, respectively. Silicon strips 60-nm thick with a width of 50 $\mu$m and a length of 250 $\mu$m were formed on quartz glass substrates.

age pulse duration and control electrical current precisely, a simple circuit was developed with a capacitance connected to silicon films in parallel, as shown by an equivalent circuit in Fig. 2(a). The electrical current flowing in the silicon films is controlled by the capacitance. If the resistances and the capacitance are constant with time in the equivalent circuit, the electrical current in silicon films at time $t$ is given by,

$$t \le T \tag{1}$$

$$I(t) = \frac{V_o}{R_l + R_{Si}} \left(1 - \frac{R_s}{R_s + R_l + R_{Si}}\right) \left(1 - \exp\left(-\frac{R_s + R_l + R_{Si}}{(R_l + R_{Si})\, R_s C} t\right)\right)$$

$$t > T$$

$$I(t) = I(T) \exp\left(-\frac{t - T}{C(R_l + R_{Si})}\right)$$

where $R_s$, $R_{Si}$ and $R_l$ are the series resistance, the resistance of silicon films and the load esistance, respectively, $C$ is the capacitance, $V_o$ is the output voltage at the voltage source and $T$ is the pulse duration of the voltage source.

Figure 2(b) shows the electrical current obtained experimentally with a capacitance of 0.22 $\mu$F as a function of time, and the current calculated using eq. (1) under the assumption that the silicon film was completely melted and had a constant and minimum resistance. The resistance of silicon was obtained by fitting the calculated current to the experimental current at a maximum value. Laser irradiation initiated an increase in the electrical current. The electrical current reached a maximum at the termination of voltage pulses at 3 $\mu$s. After that, an electrical current was still observed. Both experimental and calculated electrical currents decreased with time for a while, keeping the same current after termination of the voltage pulses. This means that the resistance of silicon films did not change because the current-induced joule heating kept the silicon at the melted state for a long time. However, the experimental electrical current started decreasing rapidly at the point indicated by an arrow in Fig. 2(b) compared with that obtained by eq. (1) with a constant $R_{Si}$. This reduction of the electrical current means an increase in the resistance of the silicon films. It indicates the solidification initiation point. Solidification initiated at 7.8 $\mu$s after termination of the 3-$\mu$s voltage, as shown in Fig. 2(b). We also determined the solidification duration to be the time difference between the solidification initiation point and the point at which the electrical current reduced to zero; it was 4.5 $\mu$s. This means that the present current-induced joule heating makes it possible to control the melt duration, the cooling rate of the silicon film and the solidification duration, which are important parameters in the crystallization of silicon films.

We estimated the cooling rate by numerical analysis of heat diffusion into the glass substrate under the condition of time-dependent joule heating. We assumed that there was no substantial supercooling and silicon was solidified at the melting point of 1412°C for every heating case. A numerical analysis of temperature change was conducted using the follwing heat flow equation,[14]

$$\delta T/\delta t = Q(T)/c\rho + \delta/\delta z\,(D\delta T/\delta z) \tag{2}$$

where $T$, $Q$, $z$ are temperature, heating energy intensity, and depth, respectively, and $c$, $\rho$, $D$ are respectively specific heat, density and heat diffusion coefficient for silicon and glass.[14,15] Because the electrical current flowing in silicon films is obtained by measuring the voltage at the load resistance, the intensity of the electrical-current-induced joule heating of silicon films per unit volume is simply expressed as

$$Q(t) = \frac{R_{Si} I(t)^2}{V} = \left(\frac{V(t)}{I_{measured}(t)} - R_l\right) \frac{I_{measured}(t)^2}{V} \tag{3}$$

where $I_{measured}$ is the electrical current obtained experimentally, as shown in Figs. 1 and 2, $V(t)$ is the calculated voltage applied at the capacitance and $V$ is the volume of the silicon strips. The heating intensity obtained using eq. (3) was used for the calculation of the cooling rate of the silicon films up

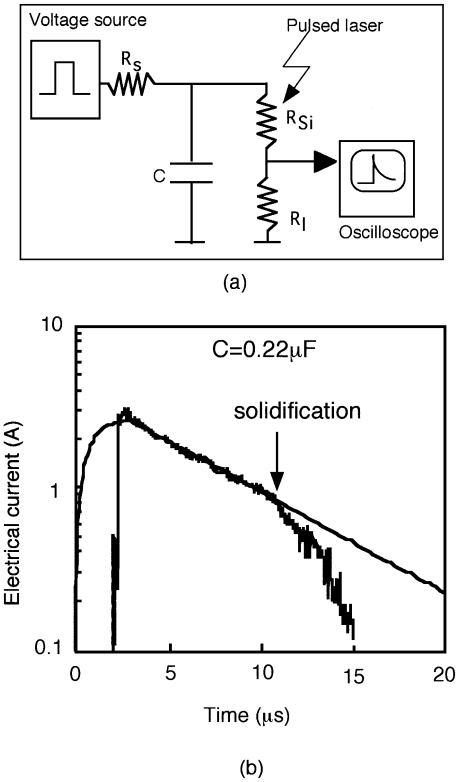


Fig. 2. Equivalent circuit with a capacitance C parallel to silicon films (a) and electrical current obtained experimentally with a capacitance of 0.22 $\mu$F as a function of time, and current calculated using eq. (1) under the assumption that the silicon films were completely melted and had a constant and minimum resistance (b). A voltage pulse at 125 V was used to obtain almost the same maximum current for the no capacitance case as that shown in Fig. 1. Arrow indicates the point at which the experimental electrical current started decreasing rapidly compared with the calculated current. Arrow indicates the solidification initiation points.

to the solidification initiation point under the assumption that silicon solidified at the melting point at the time obtained experimentally, as shown in Fig. 2(b). The cooling rate at the solidification point was estimated to be about $1.1 \times 10^8$ K/s for crystallization at a capacitance of 0.22 $\mu$F. On the other hand, the cooling rate was $6.5 \times 10^8$ K/s for crystallization at zero capacitance. The present current induced-joule heating reduced the cooling rate accompanied by an increase in melt duration. A high capacitance reduced the cooling rate to $\sim 1 \times 10^8$ K/s at the solidification point in the present conditions. In contrast, simple pulsed laser heating results in a very high cooling rate of $\sim 10^{10}$ K/s because of the very short melt duration, $<100$ ns.[16)]

Figure 3 shows the electrical conductivity as a reciprocal function of absolute temperature for $7.4 \times 10^{17}$ cm$^{-3}$ phosphorus-doped silicon films crystallized by the electrical current induced joule heating at a capacitance of 0.22 $\mu$F and at zero capacitance, as well as for simple laser crystallization at 400 mJ/cm$^2$. Al electrodes with a narrow gap of 4 $\mu$m were formed after crystallization at edge regions of silicon stripes as shown in the inset of Fig. 3. For simple laser crystallization at 400 mJ/cm$^2$, the electrical conductivity was very low at room temperature and it rapidly increased with an activation energy of 0.54 eV as the temperature increased. On the other hand, high electrical conductivities were observed for the current-induced joule heating cases and the activation energy decreased, as shown in Fig. 3. In the case of crystallization at 0.22 $\mu$F capacitance, the electrical conductivity and the activation energy were 3.5 S/cm and 0.042 eV, respectively.

We analyzed changes in the electrical conductivity of polycrystalline films using a statistical thermodynamical analysis program.[17–19)] We introduced a Gaussian-type energy distribution of the density of defect states in the band gap at grain boundaries. Phosphorus dopant atoms were assumed to be distributed uniformly in silicon films. Electron carriers are generated from the phosphorus dopant atoms via their ionization, whose probability is determined using the Fermi-Dirac statistical distribution function. Free carriers are trapped by the localized defect states and the defects are charged negatively. The Fermi energy level is determined by the statistical thermodynamical conditions maintaining the charge neutrality among the densities of ionized dopant atoms ($N_d$), defect states charged negatively with electron carriers ($X_d$) and free carriers ($n$), $N_d = n + X_d$, in the whole region including crystalline grains and grain boundaries. However, the density of ionized donors is higher than that of free electrons in crystalline grains because some electrons produced from doped phosphorus atoms are trapped at grain boundaries. This space-charge effect in crystalline grains causes band bending and results in a potential barrier at grain boundaries. We also introduced scattering effects due to dopant ions, lattice vibration and disordered states at grain boundaries, which reduced the carrier mobility.[20,21)]

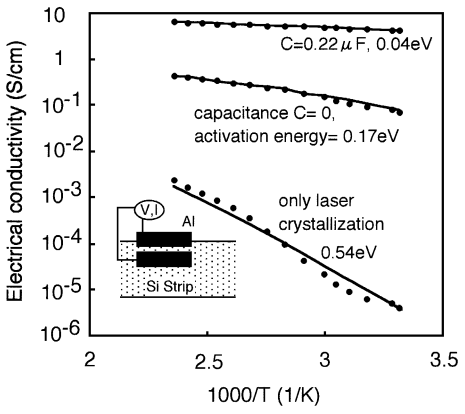


Fig. 3. Electrical conductivity measured (dotted curves) and calculated (solid curves) as a reciprocal function of absolute temperature for $7.4 \times 10^{17}$ cm$^{-3}$ phosphorus-doped silicon films crystallized by electrical-current-induced joule heating at a capacitance of 0.22 $\mu$F and at no capacitance, as well as for simple laser crystallization at 400 mJ/cm$^2$. The inset shows the image of Al electrodes with a narrow gap of 4 $\mu$m formed at the edge region of silicon strips after crystallization.

Agreement between temperature dependences of calculated and experimental conductivities revealed that planes of grain boundaries had a high defect density at $3.84 \times 10^{12}$ cm$^{-3}$ in the case of simple laser crystallization at 400 mJ/cm$^2$. In this estimation, the average grain size was 45 nm, as determined by TEM observation. For the crystallization of silicon films by electrical-current induced-joule heating, we did not determine the distribution of the crystalline grains and the number of grain boundaries in 4-mm-long electrodes; we hypothesized that there was a single grain boundary between electrodes. We introduced a numerical factor ($<1$) to obtain the effective width of the electrode for fitting the calculated electrical conductivity to the experimental one, because the electrical current must flow along the path that has the lowest number of grain boundaries or has grain boundaries with the lowest potential barrier. For crystallization at zero capacitance, the best agreement between the calculated and the experimental temperature change in the electrical conductivity gave a density of defect states per unit area at grain boundaries of $1.5 \times 10^{12}$ cm$^{-2}$, which was much lower than that of silicon films by laser crystallization. The potential barrier height at grain boundaries was 0.11 eV at room temperature. On the other hand, the calculation of temperature change in the electrical conductivity assuming no defect states showed good agreement with the experimental result for crystallization of 0.22 $\mu$F, as shown in Fig. 3. The electrical conductivity gradually increased with an activation energy of 0.042 eV as temperature increased only because the ionization probability of dopant atoms and the density of thermionic carrier increased. Single-domain crystalline regions were probably formed in the 4-mm-long electrodes via crystallization with a low cooling rate of $\sim 1.1 \times 10^8$ K/s and a long melt duration of 12 $\mu$s.

A transmission electron microscope was used for observation of the distribution of crystalline grains. Figure 4 shows a photograph of the bright-field image at the edge region of silicon stripes crystallized by the present method at a capacitance of 0.22 $\mu$F. Crystalline grains about 3.5 $\mu$m long were formed from the edge. The width of the grains was rather narrow at about 0.5 $\mu$m. Crystalline grains were formed close to each other and there is no marked disordered region among them. The preferential crystalline orientation direction to the substrate was (110). The large grain growth at the edge region indicates that crystallization probably initiated at the edge of the silicon stripes and proceeded inside. The solidification velocity was roughly estimated from the average crystallization duration of 4.5 $\mu$s and the average grain size of 3.5 $\mu$m obtained by measurements of the transient electrical current and TEM

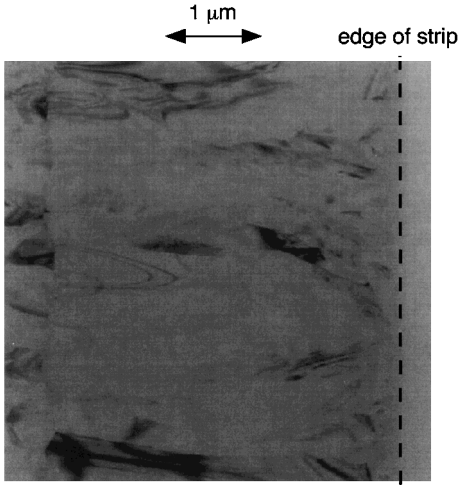


Fig. 4. Photograph of the bright-field image at the edge region of silicon stripes crystallized by the electrical-current-induced joule heating method at a capacitance of 0.22 $\mu$F and a pulsed voltage of 125 V.

observation, as shown in Figs. 2 and 4; it was about 0.8 m/s (=3.5/4.5). It is interesting that the crystallization velocity for the present method is almost the same as that for simple pulsed laser crystallization of silicon thin films formed on glass substrate,[22] although the melt duration and the cooling rate were very different between them. Optical microscopy revealed that there was no change in the film thickness during crystallization.

In summary, we investigated electrical-current-induced joule heating for the crystallization of silicon films. Pulsed voltages with a width of 3 $\mu$s and coincident irradiation with a 28-ns-pulsed excimer laser at 400 mJ/cm$^2$ were applied to 60-nm-thick amorphous silicon films formed on glass substrates and capacitance connected in parallel. A large electrical current flowed in the silicon films and joule heating melted the silicon films completely for a long time. The joule heating from electrical energy accumulated at the capacitance at 0.22 $\mu$F caused the duration of complete melting and the solidification duration to be 7.8 $\mu$s and 4.5 $\mu$s, respectively. Heat flow analysis gave the cooling rate of $1.1 \times 10^8$ K/s. For the crystallization of $7.4 \times 10^{17}$ cm$^{-3}$ phosphorus-doped silicon films, the high electrical conductivity further increased from 0.1 to 3.5 S/cm and the activation energy decreased from 0.17 to 0.042 eV as the capacitance increased from 0 to 0.22 $\mu$F when 4-$\mu$m-long electrodes were used for current measurements. Statistical thermodynamical analysis of the electrical conductivity showed that the density of the defect states at grain boundaries plane was about $1.5 \times 10^{12}$ cm$^{-2}$ and the potential barrier height at grain boundaries was 0.11 eV for crystallization at zero capacitance. Transmission electron microscopy revealed that 3.5-mm-long crystalline grains were formed at the edge regions. The grains were formed close to each other and were aligned along the silicon stripes. Preferential crystalline orientation normal to substrate was (110). These results showed the possibility of the formation of large crystalline grains with a low defect density using the electrical-current-induced joule heating method.

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1) T. Sameshima, S. Usui and M. Sekiya: IEEE Electron Device Lett. **7** (1986) 276.
2) K. Sera, F. Okumura, H. Uchida, S. Itoh, S. Kaneko and K. Hotta: IEEE Trans. Electron Devices **36** (1989) 2868.
3) T. Serikawa, S. Shirai, A. Okamoto and S. Suyama: Jpn. J. Appl. Phys. **28** (1989) L1871.
4) A. Kohno, T. Sameshima, N. Sano, M. Sekiya and M. Hara: IEEE Trans. Electron Devices **42** (1995) 251.
5) A. Matsuda: J. Non-Cryst. Solids **59/60** (1983) 767.
6) Y. Chida, M. Kondo and A. Matsuda: J. Non-Cryst. Solids **198-200** (1996) 1121.
7) K. Nakahata, A. Miida, T. Kamiya, Y. Maeda, C. M. Fortmann and I. Shimizu: Jpn. J. Appl. Phys. **37** (1998) L1026.
8) H. Matsumura: Jpn. J. Appl. Phys. **37** (1998) 3175.
9) K. H. Lee, J. K. Park and J. Jang: IEEE Trans. Electron Devices **45** (1998) 2548.
10) H. Kuriyama, T. Kuwahara, S. Ishida, T. Nohda, K. Sano, H. Iwata, S. Noguchi, S. Kiyama, S. Tsuda, S. Nakano, M. Osumi and Y. Kuwano: Jpn. J. Appl. Phys. **31** (1992) 4550.
11) T. Sameshima: Jpn. J. Appl. Phys. **32** (1993) L1485.
12) J. S. Im and H. J. Kim: Appl. Phys. Lett. **64** (1994) 2303.
13) R. Ishihara, W.-C. Yeh, T. Hattori and M. Matsumura: Jpn. J. Appl. Phys. **34** (1995) 1759.
14) R. F. Wood and G. E. Giles: Phys. Rev. B **23** (1981) 2923.
15) A. Goldsmith, T. E. Waterman and H. J. Hirschorn: *Handbook of Thermophysical Properties of Solid Materials* (Pergamon Press, New York, 1961) Vols. 1 and 3.
16) S. R. Stiffler, M. O. Thompson and P. S. Peercy: Phys. Rev. B **43** (1991) 9851.
17) J. Y. W. Seto: J. Appl. Phys. **46** (1975) 5247.
18) K. Sakamoto, T. Sameshima, Y. Tsunoda and S. Higashi: *Proc. Workshop on Active Matrix Liquid Crystal Displays, Tokyo, 1999* (Jpn. Soc. Appl. Phys., Tokyo, 1999) p. 131.
19) G. Baccarani, B. Ricco and G. Spadini: J. Appl. Phys. **49** (1978) 5565.
20) J. C. Irvin: Bell Syst. Tech. J. **41** (1962) 387.
21) M. B. Prince: Phys. Rev. **94** (1954) 42.
22) T. Sameshima, M. Hara and S. Usui: Jpn. J. Appl. Phys. **28** (1989) 1789.