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Measurements of Temperature Distribution in Polycrystalline Thin Film Transistors Caused by Self-Heating

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Transient thermometry was applied to measure temperature distribution caused by self-heating in n-channel poly-Si TFTs on glass. Pt wires 30 nm thick were formed above the Al gate electrode via an intermediate SiO_2 layer with positions above the drain edge, middle and the source as temperature sensors. Temperature above the drain edge increased 9 K from room temperature at a power consumption of 20 μW/μm per unit gate width, while it increased only 6 K above the source edge when the TFT was operated in a saturation mode. This results from heat generation being localized near the drain edge. The temperature change with time is also discussed.

KEYWORDS: transient thermometry, laser crystallization, heat diffusion

Polycrystalline silicon thin film transistors (poly-Si TFTs) are important for many electrical device applications, especially for liquid crystal displays (LCD) and static random access memories (SRAM) because they have high drive currents and both n- and p-channel TFTs can be realized.[1–4] But the low thermal conductivity of glass substrate can cause self-heating of TFTs during operation. The self-heating effect may reduce TFT performances, for example, the leakage current or the drain saturation current. The self-heating also increases the temperature of surrounding regions, particulary in integrated circuits with a high density of TFTs operated with a high current. Three-dimensional heat flow calculations have been carried out to determine temperature distribution in transistors.[5] A silicon temperature sensor has been used to observe the self-heating effect, especially in power metal oxide semiconductor field effect transistors.[5–7] However, the heat capacity of the temperature sensor must be reduced in order to measure change in temperature in TFTs accurately because film layers of TFTs are thin only about 100 nm. If the temperature sensor is thick, the temperature measured in TFTs may be inaccurate due to heat diffusion into the sensor.

We report measurements of self-heating-induced temperature distribution in poly-Si TFTs fabricated on glass substrates. A thin Pt temperature sensor[8] with a thickness of 30 nm enables precise measurements of change in temperature with time and different operation modes of TFTs.

N-channel poly-Si TFTs with a gate width of 500 μm and a length of 100 μm were fabricated on a glass substrate. Islands of 20-nm-thick hydrogenated amorphous silicon films doped with 2-at%-phosphorus were first formed on a glass substrate at 250°C using conventional plasma-enhanced chemical vapor deposition (PECVD) and an SF_6-plasma etching method as a dopant source for forming source and drain regions. A 20-nm-thick undoped a-Si:H film was then deposited using PECVD over the whole area. Island patterning was conducted by etching the amorphous layers. The silicon layers were crystallized by 30-ns-pulsed XeCl excimer laser irradiation in vacuum with an energy of 210 mJ/cm^2 to form the undoped poly-Si and doped poly-Si formed by diffusion of dopant atoms during melting. After irradiation, the silicon layers were hydrogenated using hydrogen plasma with RF popwer of 5 W for 30 s at 270°C in order to reduce the density of defect states.[9] SiO_2 films 200 nm thick were deposited by remote plasma chemical vapor deposition (RPCVD)[10] with SiH_4 and O_2 gas mixture with a RF power of 5 W at 270°C. Contact holes were formed in the SiO_2 layers at the source and drain regions for both TFT's. The Al gate, source and drain electrodes were then formed. SiO_2 films 200 nm thick were again deposited over the whole area as an intermediate layer for temperature measurements. Pt wires 30 nm-thick with a width of 20 μm and a length of 500 μm were formed above the channel region of TFTs as a temperature sensor via the SiO_2 layer using a lift-off method at positions on the drain edge, the source edge and middle, respectively, as shown in Fig. 1. Al lines 100 nm thick and 30 μm wide were formed outside TFTs and connected to the Pt lines in order to reduce the series resistivity. Contact holes were formed in the intermediate SiO_2 layer on the drain, source and gate electrodes. TFT's were then annealed at 300°C for 1 h in H_2O vapor atmosphere, in order to improve the electrical properties of SiO_2 and the SiO_2/poly-Si interface.[11]

Output and transfer characteristics of the TFTs were measured to check good ohmic characteristics, the threshold voltage and the carrier mobility. They were 2 V and 140 cm^2/Vs which was obtained at the drain voltage of 5 V and the gate voltage of 12 V. Before temperature measurements, the relationship between the resis-

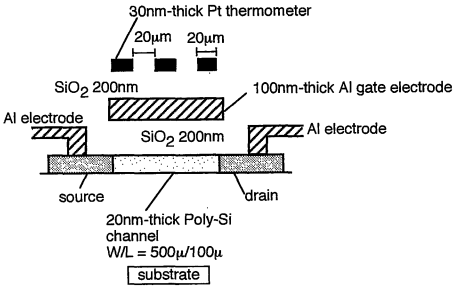

Fig. 1. Cross section of poly-Si TFT and Pt temperature sensor.

tivity of Pt wires and their temperature was determined by measuring the change in the resistivity of Pt wires when the samples were placed on a heating plate whose temperature was changed carefully from 20 to 50°C using a current heater. A voltage of 0.2 V was applied to the Pt wires for the resistivity measurements because the resistivity of Pt was not changed by self-heating of Pt itself when the applied voltage was lower than 2 V. Afterwards, the change in resistivity of Pt wires caused by heat diffusion from TFTs self-heated during their operation was measured with a time resolution of 0.01 s and an interval of 0.05 s at room temperature.

Figure 2 shows the normalized temperature increase of the Pt wires located above the drain edge, the middle and the source edge as a function of time during and after the application of a voltage of 12 V to both the drain and the gate for 2 s. The normalized temperature increase means the temperature increase divided by the maximum increase measured for each Pt wire. Thus, it is zero before TFT operation and one at the maximum temperature. The temperature increased by 6.5 K for Pt above the drain edge, 5.3 K for the middle, and 4.4 K above the source edge. The temperature of Pt above the drain edge increased rapidly and reached the maximum at 0.15 s. The temperature of Pt above the source edge increased more slowly and took 0.45 s to reach the maximum. The TFT's ON state was in a saturation mode, in which the drain current is independent of the drain voltage and the most of voltage drop in the channel occurs near drain edge.[12] The power consumption and heat generation occur in a limited region close to the drain. It therefore takes a longer time for the temperature of Pt above the source edge to become saturated because this Pt is far from the heating region (~100 μm) compared with Pt above the drain edge and heat diffusion requires a longer time.

Figure 3 shows the increment of saturated temperatures as a function of power consumption per unit gate width (μW/μm) of the TFT for the Pt wires above the drain and source edges. For each power consumption, the temperature was measured at 2 s after the application of drain and gate voltages, which gave the TFT ON state in saturation ($V_g = V_d$) as well as linear ($V_g = 3V_d$) modes. The temperature increased linearly with increasing the power consumption for the every Pt wire. For the Pt wire above the drain edge, the temperature for the TFT's saturation mode increased with slightly higher rate than that in the case of the linear mode and it increased 9 K from room temperature at 20 μW/μm (10 mW). The Pt sensor above the drain edge is heated more effectively because the power consumption region is localized just below the Pt wire for the TFT's saturation mode, while it extends over the whole channel region for the linear mode. In contrast, for the Pt wire above the source edge, the rate of temperature increasing for the saturation mode was lower than that for the linear mode which was almost the same rate of temperature change of the Pt above the drain edge for the linear mode as shown in Fig. 3. The temperature increased only 6 K from room temperature at 20 μW/μm. This result means that the Pt wire is heated less than in the case of the linear mode

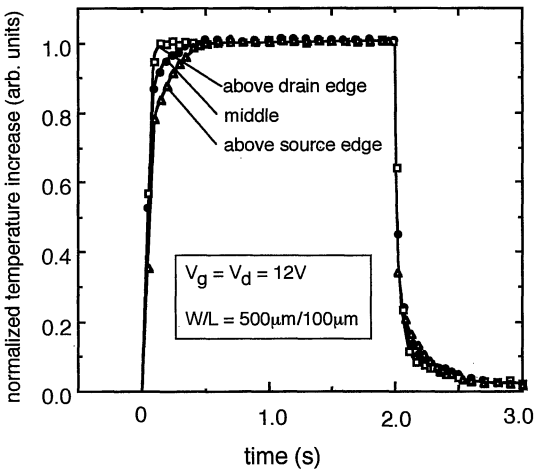

Fig. 2. Change in normalized temperature increase of Pt above drain edge, middle and source edge while a voltage of 12 V was applied to both the gate and drain electrodes (saturation mode) for two seconds.

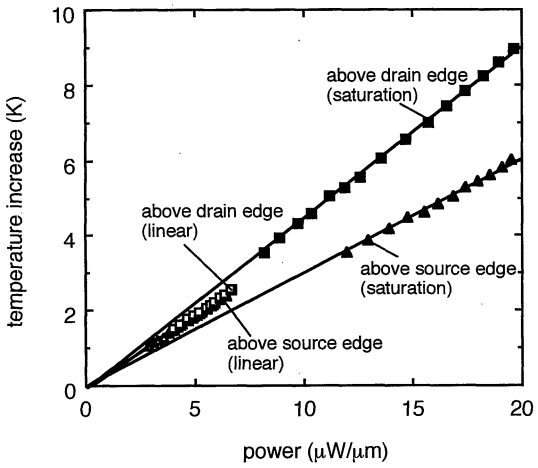

Fig. 3. Change in temperature increase of Pt above the drain edge and source edge as a function of power consumption when the TFT was operated with $V_g = V_d$ (saturation mode) as well as $V_g = 3V_d$ (linear mode).

operation because the Pt wire above the source edge is far from the self-heating region for the saturation mode, although the poly-Si layer and the Al gate formed below the Pt wires can result in lateral heat diffusion.

The results in Figs. 2 and 3 show that the present system enables precise measurements of temperature change caused by self-heating of TFTs. Heat diffusion is complicated in general because of the layered structures of TFTs and surrounding metal electrodes. There are many three-dimensional heat diffusion paths. Temperature change also depends on the channel length because the distribution of power consumption and heat generation regions changes with the channel length. The present temperature measurement system would be useful for measuring temperature change with time and temperature distribution caused by self-heating in complicated electrical circuit structures.

In summary, thin Pt wires with a thickness of 30 nm were used to precisely measure the temperature increase

above the channel region caused by self-heating of n-channel Al gate poly-Si TFTs with the gate width of 500 μm, the gate length of 100 μm, the poly-Si thickness of 20 nm and 200-nm-thick SiO_2 gate insulator. Temperatures above the drain edge and the source edge reached maximum values at 0.15 s and 0.45 s, respectively, for TFT saturation mode operation because of the localization of the heat generation region close to the drain. The temperature above the drain edge increased 9 K from room temperature at a power consumption of 20 μW/μm per unit gate width for the saturation mode operation. It is found that the temperature distribution depends on the TFT operation mode because the heat generation region is localized at the drain edge for the saturation mode whereas it extends over the channel for the linear mode. The present method would be useful for heat flow analysis especially in complicated integrated circuits.

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